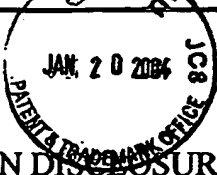
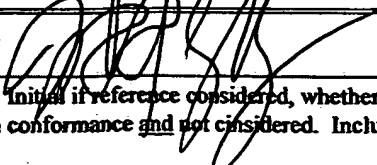


Form PTO-1449 (Modified)		U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. 20002/17225	Serial No. 10/677,414
<b>INFORMATION DISCLOSURE STATEMENT</b> (Use several sheets if necessary)			Applicant TIAN et al.	
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U.S. PATENT DOCUMENTS							
*EXAMINER INITIALS	DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	

FOREIGN PATENT DOCUMENTS							
*Examiner Initials	Document Number	Publication Date	Country	Class	Subclass	Translation Yes No	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)		
TH	✓	M. Annavaram, J. Patel, E. Davidson. Data Prefetching by Dependence Graph Precomputation. In 28 <sup>th</sup> International Symposium on Computer Architecture, Goteborg, Sweden, July 2001.
	✓	M. Carlisle. Olden: Parallelizing Programs with Dynamic Data Structures on Distributed-Memory Machines, <i>Ph.D. Thesis</i> , Princeton University Department of Computer Science, June 1996.
	✓	R. Chappell, J. Stark, S. Kime, S. Reinhardt, and Y. Patt. Simultaneous Subordinate Microthreading (SSMT). In 26 <sup>th</sup> International Symposium on Computer Architecture, May 1999.
	✓	J. Collins, H. Wang, D. Tullsen, C. Hughes, Y. Lee, D. Lavery, J. Shen. Speculative Precomputation: Long-range Prefetching of Delinquent Loads. In 28 <sup>th</sup> International Symposium on Computer Architecture, Goteborg, Sweden, July 2001.
	✓	Intel Corporation. "Intel delivers Hyper-Threading Technology with Pentium 4 Processor 3 Ghz milestone." <a href="http://www.intel.com/pressroom/archive/release/20021114comp.htm">http://www.intel.com/pressroom/archive/release/20021114comp.htm</a> . As printed on Jan. 12, 2003.
TH	✓	D. Kim and D. Yeung. Design and Evaluation of Compiler Algorithms for Pre-Execution. In ASPLOS-X Conference, pp. 159-170, October 2002.

EXAMINER 	DATE CONSIDERED 3/26/07
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<p align="center"><b>INFORMATION DISCLOSURE STATEMENT</b></p> <p align="center">(Use several sheets if necessary)</p>		Applicant TIAN et al.	
		Filing Date 10/02/03	Group Art Unit 2121 2193

TX	S. Liao, P. Wang, H. Wang, G. Hoflehner, D. Lavery, J. Shen. "Post-Pass Binary Adaption For Software-Based Speculative Precomputation." Proceedings of the ACM SIGPLAN 2002 Conference On Programming Language Design And Implementation. 2002.
	H. Wang, P. Wange, R. Weldon, S. Ettinger, H. Saito, M. Girkar, S. Liao, J. Shen. Speculative Precomputation: Exploring the Use of Multithreading for Latency. In <i>Intel Techonology Journal</i> Q1, 2002. Vol. 6 Issue 1.
TX	X. Tian, A. Bik, M. Girkar, P. Grey, H. Saito, E. Su. Intel OpenMP C++/Fortran Compiler for Hyper-Threading Technology: Implementation and Performance. In <i>Intel Technology Journal</i> Q1, 2002. Vol. 6 Issue 1.

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Intel/17225

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10/677,414

Applicant

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Filing Date

October 2, 2003

Group Art Unit

2121

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SUPPLEMENTAL INFORMATION DISCLOSURE  
STATEMENT

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## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

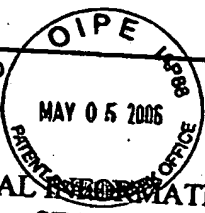
CP	C01	International Search Report for International application no. PCT/US2004/032212 published with publication no. WO 2005/033926 A3, April 14, 2005
EP	C02	Dorai et al., <i>Optimizing SMT Processors for High Single-Thread Performance</i> , Journal of Instruction Level Parallelism 5 (2003), April 2003, pp 1-35.

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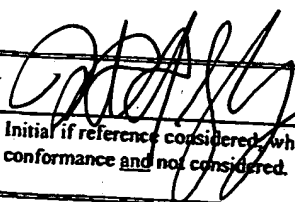
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			Applicant <b>Tian et al.</b>	
			Filing Date <b>October 2, 2003</b>	Group Art Unit <b>2121-2193</b>

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)		
<i>TJ</i>	C01	Submitted herewith is a copy of a Written Opinion of the International Searching Authority for the International application no. PCT/US2004/032212.
	C02	

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